PVP 14

Code: EC5T3

III B.Tech - I Semester – Regular/Supplementary Examinations
October 2019

COMPUTER ARCHITECTURE AND ORGANIZATION
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1. a) What is register transfer language? Give an example for RTL.
   b) Define bus and list the types.
   c) What is the function of control memory?
   d) Define Micro-operation.
   e) Differentiate isolated I/O and Memory mapped I/O.
   f) What is content addressable memory?
   g) Perform the (+21) + (-16) arithmetic operations using 2's complement representation for negative numbers.
   h) What is the need of normalization for floating point numbers?
   i) Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow.
   j) What is pipelining? Draw the diagram for instruction pipelining.
   k) Write down the expressions for speedup factor in a pipelined architecture.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) What are functional units? Discuss on basic functional units of a computer? 8 M

   b) What is instruction cycle? Explain each phase of instruction cycle with neat diagram? 8 M

3. a) Explain about microinstruction sequencing techniques, specifically variable format address microinstruction. 8 M

   b) Give the major characteristics of RISC and CISC architectures. 8 M

4. a) With a neat diagram, describe DMA transfer in a computer system. 8 M

   b) Discuss about Auxiliary memory and Cache memory. 8 M

5. a) Derive and explain an algorithm for adding and subtracting two floating point binary numbers. 8 M

   b) Explain the process of multiplying binary integers with Booth's algorithm. 8 M

6. a) What is parallel processing? What are its advantages? Explain. 8 M

   b) Explain vector processing. 8 M